REMARKS

Upon entry of the instant amendment, claims 1-23 will be pending. Claims 1, 3, 4, 6-9, 11-13, and 15-21 have been amended, and new claims 22-23 have been added. No new matter has been introduced. An action on the merits is respectfully requested.

In the Office Action dated February 14, 2006 (hereinafter referred to simply as the "Office Action"), the Examiner rejected:

> (1) Claims 1-7, 10-12, and 14-21 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,248,945 to Sasaki (hereinafter referred to as "Sasaki"), in view of U.S. Patent No. 5,902,949 to Mohrbacher (hereinafter referred to as "Mohrbacher");
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> (2) Claims 8-9 and 13 under 35 U.S.C. § 103(a) as being unpatentable over Sasaki and Mohrbacher, in further view of U.S. Patent No. 5,339,311 to Turner (hereinafter referred to as "Turner"); and
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> (3) Claims 1-6, 12-15 and 19-21 under 35 U.S.C. § 112 as being indefinite.

These rejections are respectfully traversed with respect to the claims as amended, as well as the new claims submitted, herein.

The present invention is directed to a system (and corresponding method, computer-readable medium, etc.) for providing packet communications between a server and a client by way of a network, such as, e.g., the Internet. The server inputs data, such as MIDI data, in a sporadic manner, while storing timing data representing the respective input timing of each piece of input data. The server then packetizes the sporadically input data, which accompany the timing data and are transmitted to the client.

The client, in turn, receives the packetized input data and then outputs them, as output data, at timings based on the input timing data, such that the time interval between two consecutive pieces of output data is the same as the time interval between the two consecutive pieces of (sporadically) input data corresponding to the two pieces of output data. In this way, the time relationship of data during transmission and reception of the sporadically input data is preserved. That is, the original time information representing respective time intervals of (input) data is reproduced upon outputting of the data.

In embodiments of the invention, the timing data (or information) is represented by a series of bits. Thus, in one embodiment, shown generally in Figures 3A and 3B of the instant application as filed, timing data is expressed by an 8-bit shift register, wherein the designation of a "1" in a specific bit position indicates the specific timing at which a piece of data has been input. Similarly, a "0" in a specific bit position indicates that no data has been input (and, therefore, that no data is stored in the buffer register of the RAM 24).

Thus, in the example shown in Figure 3A, e.g., packet timings tn-1, tn, tn+1, tn+2, and tn+3 consecutively occur on the time axis. The server 3 inputs data D1 and D2 during a packet timing interval between the packet timings tn-1 and tn, during which digits "1" and "0" are accumulated in eight bits of timing data Dtn. The input data D1 and D2 (e.g., MIDI data) accompanying the timing data Dtn are collectively transmitted at the packet timing tn. As shown, the timing data Dtn reads "00010010", which indicates that the data D1 is input at a timing corresponding to the fourth bit counted from the leftmost bit, and the data D2 is input at a timing corresponding to the seventh bit.

Where no data is input to the server 3 at all in the period between the packet timing tn and the packet timing tn+1, eight bits of timing data are all set to zero. At the packet timing tn+1, the timing data whose binary notation is "00000000" are stored in the timing data register. At this time, the buffer register of the RAM 24 stores no data to be transmitted from the server 3 to the client 9.

During the next packet timing interval between packet timings tn+1 and tn+2, the server 3 inputs data D3 and D4, which are stored in the buffer register of the RAM 24 so that the timing data register stores corresponding timing data Dtn+2. The input data D3 and D4 accompanying the timing data Dtn+2 are collectively transmitted at the packet timing tn+2. Thus, the timing data Dtn+2 reads "01000100", which indicates that the data D3 is input at a timing corresponding to the second bit counted from the leftmost bit, and the data D4 is input at a timing corresponding to the sixth bit.

In this way, the server 3 proceeds to collectively transmit the packet corresponding to the combination of the data D1 and D2 accompanying the timing data Dtn at the packet timing tn, followed by collective transmission of the packet corresponding to the combination of the data D3 and D4 accompanying the timing data Dtn+2 at the packet timing tn+2. Thus, the server 3 packetizes the input data (e.g., MIDI data) and timing data at each packet timing and transmits the packetized data to the client 9 over a network 40.

The client 9, in turn, receives the packetized data consisting of the input data and timing data by means of a communication interface 31, and proceeds to separate the input data and timing data. That is, the timing data are stored in the timing data register of the RAM 24, while the received data (i.e., received MIDI data) are stored in the buffer register of the RAM 24.

When a "1" is output from the timing data register, the client 9 reads and outputs one data from the buffer register of the RAM 24. Therefore, each of the received data is to be output from the client 9 in accordance with a corresponding "1" from the timing data register. In this way, the client 9 outputs each piece of received data (to a sound source 10) in complete synchronization with the prescribed timing that substantially corresponds to the timing at which the sever 3 inputs each data by the packet timing.

Using the example of Figure 3A, and with reference to Figure 3B, as noted above, the server 3 inputs the data D1 at the fourth shift timing counted from the packet timing tn-1; then, it inputs the data D2 at the seventh shift timing. These pieces of data D1 and D2 are transmitted to the client 9, wherein they are stored in the RAM 24 in connection with the timing data Dtn. Thereafter, the client 9 outputs the data D1 at the fourth shift timing that is counted from the prescribed packet timing substantially matching the packet timing tn-1. Then, the client outputs the data D2 at the seventh shift timing.

Similarly, the server 3 inputs the data D3 at the second shift timing counted from the packet timing tn+1; then, it inputs the data D4 at the sixth shift timing. These pieces of data D3 and D4 are transmitted to the client 9, wherein they are stored in the RAM 24 in connection with the timing data Dtn+2. Thereafter, the client 9 outputs the data D3 at the second shift timing that is counted from the prescribed packet timing substantially matching the packet timing tn+1. Then, the client outputs the data D4 at the sixth shift timing. Therefore, an original time interval between the input data D1 and D2, as well as D3 and D4, respectively, input to the server 3 is completely preserved in the client 9, which outputs the data D1 and D2, as well as D3 and D4, respectively, to the sound source 10.

Claim 1, as amended herein, recites (emphases added):

> 1. A communication method that is executed by a transmission unit and a reception unit, comprising:
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> packetizing one or more items of sporadically input data to accompany timing information representing respective input timings of the one or more items of sporadically input data, said timing information being in the form of a plurality of bits, wherein:
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> each one of said plurality of bits is periodically produced and takes on either a first binary value or a second binary value that is different from the first binary value; and
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> for each periodically-produced bit, a bit value equal to the first binary value represents a timing at which one of said items of sporadically input data is inputted to the transmission unit, and a bit value equal to the second binary value represents a timing at which no data is inputted to the transmission unit;
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> transmitting the packetized data along with the timing information from the transmission unit;
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> receiving the packetized data along with the timing information by the reception unit; and
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> outputting the packetized data as output data at timings based on the timing information from the reception unit, wherein, for each bit of the received timing information, when the bit value is equal to the first binary value, a corresponding item of the packetized data is outputted by the reception unit, and when the bit value is equal to the second binary value, no data is outputted by the reception unit, such that respective timings of the output data correspond to said respective input timings of the sporadically input data.

In the Office Action, the Examiner initially states (and subsequently, in rejecting claim 1, essentially re-asserts) that "Sasaki does indeed disclose utilizing bits as a means to keep track of input timings [column 7, <<lines 57-60>>]". *See* Office Action, p. 3; *see also* Id., Par. 9. More specifically, the Examiner asserts that:

> Bits comprise bytes, and thus by implication, Sasaki discloses bits within his invention in dealing with timing of the input data. Furthermore, a register is well known in the art as being a memory for storing information in byte form. Thus,

Sasaki's time register, also by implication, discloses utilizing bits to store timing information.

The section of Sasaki that is cited by Examiner provides that (*see* Sasaki, col. 7, lines 57-61):

> The time data to be added to the MIDI data is assumed having 4 bytes representing a time, for example, with a unit of millisecond. Therefore, when MIDI data is transmitted as the music information, the data quantity is of 8 bytes in total.

It is respectfully submitted that even if, *arguendo*, Sasaki's mere reference to "bytes" were sufficient to create a basis for establishing that Sasaki teaches representation of respective timing data in bit format, Sasaki does not disclose, teach, or even remotely suggest, the recitation in amended claim 1 of "timing information being in the form of a plurality of bits, wherein: each one of said plurality of bits is periodically produced and takes on either a first binary value or a second binary value that is different from the first binary value; and for each periodically-produced bit, a bit value equal to the first binary value represents a timing at which one of said items of sporadically input data is inputted to the transmission unit, and a bit value equal to the second binary value represents a timing at which no data is inputted to the transmission unit".

Similarly, Sasaki fails to disclose, teach, or even remotely suggest "when the bit value is equal to the first binary value, a corresponding item of the packetized data is outputted by the reception unit, and when the bit value is equal to the second binary value, no data is outputted by the reception unit, such that respective timings of the output data correspond to said respective input timings of the sporadically input data".

More specifically, claim 1, as amended, requires that timing information associated with data (such as, e.g., MIDI data) be indicated by a set of binary values, wherein a bit value equal to

a first binary value (e.g., a "1") represents the existence of input/output data (e.g., MIDI data) associated with that bit (i.e., time) position, and wherein a bit value equal to a second binary value (e.g., a "0") represents the absence of input/output data associated with the bit position. The above is not disclosed, taught, or even alluded to in Sasaki.

Recognizing this shortcoming, in rejecting claim 1, the Examiner cites to col. 53, line 34-col. 54, line 32 of Mohrbacher, and states that (*see* Office Action, Par. 9, pp. 4-5):

> Mohrbacher discloses said timing information being represented by a series of bits, wherein, within a given time interval, a bit value of "1" indicates an input timing for a specific piece of input data [].
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> Mohrbacher utilizes the input timing information to signify the when [sic] each note must be played relative to other notes within the composition, hence, a 'relative time stamp'. As seen in the table, Mohrbacher discloses a time stamp represented by a series of bits. It is well known in the art to use "1" or a "0" within a byte structure to convey information.

The section of Mohrbacher that is cited by the Examiner provides, in relevant part, as follows (*see* col. 53, lines 34 – 52; emphases added):

> Referring now in more detail to song block keycode performance data format 422 in FIG. 29, the first byte of the 4 byte performance data is the byte which identifies the time of occurrence of the byte. To minimize data storage and bandwidth requirements, the time of occurrence is provided by a number which represent the relative time of the occurrence from the previous note. The number represents the number of ticks of a time clock such as music time clock 284, shown in FIG. 11. Music time clock 284 represents a music time clock within music controller portion 102b which used [sic] to determine the time of occurrence of each event from the time at which the performance was begun. That is, the time clock is reset to a beginning time, such as zero ticks, and all time is made relative to that time by using time stamps which represent the count from zero.
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> The time of occurrence is therefore represented by a relative time stamp, such as <RelTimeStamp> data byte 424, providing delta or differential time information (as shown below in TABLE I by the letter code d).

As is evident from the above-quoted passages, Mohrbacher discloses a system in which the time information is progressive and, as such, is "relative" to an absolute (zero) time. In addition, contrary to the Examiner's assertion, Table I does not teach the use of a "1" or "0" in its "time stamp". In fact, if anything, Mohrbacher teaches against such usage, because, as shown in Table I, each "bit" position is occupied by a "d", which the reference itself defines as "delta or differential time information."

Put another way, because of its structure, at best, Mohrbacher's system shows, *arguendo*, only the existence of data by the value of its bit positions, because each succeeding bit position indicates the timing of the next event. Thus, because all of the succeeding bits contain "delta" time information, i.e., the time to the next event, none of the bit positions can indicate the absence of an event (i.e., the absence of data). However, as noted above, the latter is a positive limitation of amended claim 1, wherein "a bit value equal to the second binary value represents a timing at which no data is inputted", and "when the bit value is equal to the second binary value, no data is outputted".

Therefore, it is respectfully submitted that Mohrbacher does not disclose, teach, or suggest *packetizing one or more items of sporadically input data to accompany timing information representing respective input timings of the one or more items of sporadically input data, said timing information being in the form of a plurality of bits, wherein: each one of said plurality of bits is periodically produced and takes on either a first binary value or a second binary value that is different from the first binary value; and for each periodically-produced bit, a bit value equal to the first binary value represents a timing at which one of said items of sporadically input data is inputted to the transmission unit, and a bit value equal to the second binary value represents a timing at which no data is inputted to the transmission unit;*

transmitting the packetized data along with the timing information from the transmission unit; receiving the packetized data along with the timing information by the reception unit; and outputting the packetized data as output data at timings based on the timing information from the reception unit, wherein, for each bit of the received timing information, when the bit value is equal to the first binary value, a corresponding item of the packetized data is outputted by the reception unit, and when the bit value is equal to the second binary value, no data is outputted by the reception unit, such that respective timings of the output data correspond to said respective input timings of the sporadically input data.

In light of the above, and given that Turner does not rectify the shortcomings of Sasaki and Mohrbacher, it is respectfully submitted that the cited references do not disclose, suggest, or teach, either individually or in combination, all of the limitations of claim 1, as amended. The Applicants therefore respectfully submit that amended claim 1 distinguishes over the cited art and is in condition for allowance. As such, it is respectfully requested that the rejection of claim 1 under 35 U.S.C. § 103(a) be withdrawn.

Each of independent claims 4, 7, 12, 16, and 19 has also been amended herein to include limitations similar to those discussed above in connection with claim 1. As such, and in light of the above discussion, it is respectfully submitted that claims 4, 7, 12, 16, and 19 distinguish over the cited references for at least the same reasons as those noted above in connection with amended claim 1. The Applicants therefore respectfully request that the rejections (under 35 U.S.C. § 103(a)) as to claims 4, 7, 12, 16, and 19 be withdrawn, as these claims are now believed to be in condition for allowance.

In addition, claims 2-3 depend directly from claim 1, claims 5-6 depend directly from claim 4, claims 8-11 and new claim 22 depend directly from claim 7, claims 13-15 and new claim 23 depend directly from claim 12, claims 17-18 depend directly from claim 16, and claims 20-21 depend directly from claim 19. As such, it is respectfully submitted that claims 2-3, 5-6, 8-11, 13-15, 17-18, and 20-23 also distinguish over the cited art for at least the same reasons as those noted above in connection with amended claim 1. Therefore, the Applicants respectfully request that the rejection of claims 2-3, 5-6, 8-11, 13-15, 17-18, and 20-21 (under 35 U.S.C. § 103(a)) be withdrawn, as these claims are also believed to be in condition for allowance.

Finally, it is respectfully submitted that, in light of the amendments made to claims 1, 4, 12, and 19 herein, the rejection of claims 1-6, 12-15, and 19-21 under 35 U.S.C. §112, second paragraph is moot and, as such, should be withdrawn.

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It is believed that claims 1-21, as amended herein, as well as new claims 22 and 23, are in condition for allowance, and a favorable action is respectfully requested. If, for any reason, the Examiner finds the application other than in condition for allowance, the Examiner is requested to call one of the undersigned attorneys at the Los Angeles, California telephone number (213) 488-7100 to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted,
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